CY803/802 Datasheet

300M-450MHz RF receiver

General Description

The CY803/802 is a general purpose, 3.3-5V, super-heterodyne Receiver that operates from 300M to 450MHz with typical sensitivity of -110dBm. The CY803/802 functions as a super-heterodyne receiver for OOK and ASK modulation up to 10kbps.The down-conversion mixer also provides image rejection. All post-detection data filtering is provided on the CY803/802. Any one-of-four filter bandwidths may be selected externally by the user in binary steps, from 1.25kHz to 10kHz. The user need only configure the device with a set of easily determined values, based upon data rate, code modulation format, and desired duty-cycle operation.

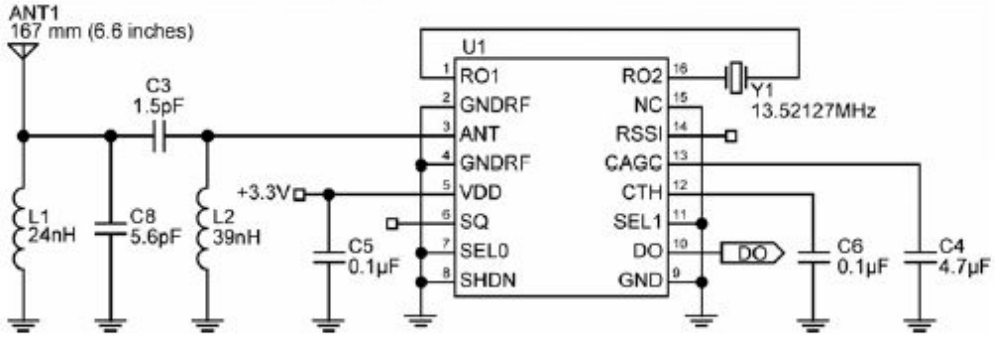
Features

- Image Rejection Mixer
  Frequency from 300MHz to 450MHz
- Low power, 6.0mA @ 433.92MHz, continuous on
- data rates to 10kbps (Manchester Encoded)
- High sensitivity: -110dBm
- No IF filter required
- Excellent selectivity and noise rejection
- Low external part count

Ordering Information

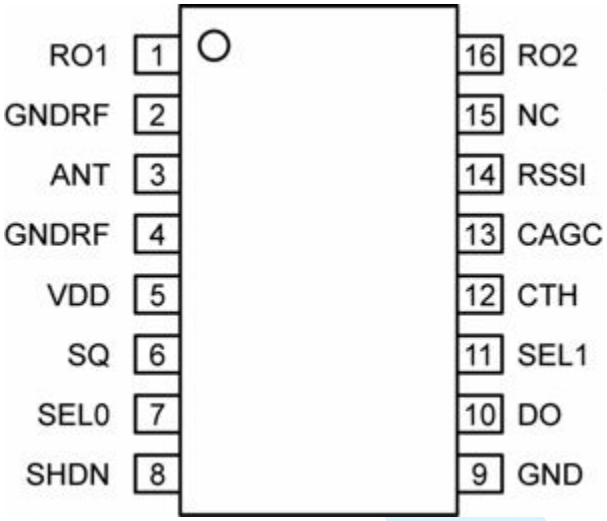
Part Number	Temperature Range	Package
CY802	–20° to +70°C	16-Pin SOP
CY803	–20° to +70°C	16-Pin SSOP

Typical Application



433.92 MHz, 1kHz Baud Rate Example

Pin Configuration



Pin Description

16-Pin QSOP	Pin Name	Pin Function
1	RO1	Reference resonator input connection to Colpitts oscillator stage. May also be driven by external reference signal of 1.5V p-p amplitude maximum.
2	GNDRF	Negative supply connection associated with ANT RF input.
3	ANT	RF signal input from antenna. Internally AC coupled. It is recommended that a matching network with an inductor -to-RF ground is used to improve ESD protection.
4	GNDRF	Negative supply connection associated with ANT RF input.
5	VDD	Positive supply connection for all chip functions.
6	SQ	Squelch control logic input with an active internal pull-up when not shut down.
7	SEL0	Logic control input with active internal pull-up. Used in conjunction with SEL1 to control the demodulator low pass filter bandwidth. (See filter table for SEL0 and SEL1 in application section)
8	SHDN	Shutdown logic control input. Active internal pull-up.
9	GND	Negative supply connection for all chip functions except RF input.
10	DO	Demodulated data output.
11	SEL1	Logic control input with active internal pull-up. Used in conjunction with SEL0 to control the demodulator low pass filter bandwidth. (See filter table for SEL0 and SEL1 in application section)
12	CTH	Demodulation threshold voltage integration capacitor connection. Tie an external capacitor across CTH pin and GND to set the settling time for the demodulation data slicing level. Values above 1nF are recommended and should be optimized for data rate and data profile.
13	CAGC	AGC filter capacitor connection. CAGC capacitor, normally greater than 0.47μF, is connected from this pin to GND
14	RSSI	Received signal strength indication output. Output is from a buffer with 200Ω typical output impedance.
15	NC	Not Connected (Connect to Ground)
16	RO2	Reference resonator input connection to Colpitts oscillator stage, 7pF, in parallel with low resistance MOS switch-to-GND, during normal operation. Driven by startup excitation circuit during the internal startup control sequence.

Absolute Maximum Ratings(1)

Supply Voltage（VDD) .....+5V

Input Voltage .....+5V

Junction Temperature .....+150ºC

Lead Temperature (soldering, 10sec.) ..... 260°C

Storage Temperature (TS) .....-65ºC to +150°C

Maximum Receiver Input Power .....+10dBm

ESD Rating（3) ..... 2KV CDM

.....200V HBM

..... 100V Machine Model

Operating Ratings(2)

Supply voltage (VDD) .....+3.3V to +5.5V

Ambient Temperature (TA) ..... –20°C to +70°C

Input Voltage (VIN) .....5.5V (Max)

Maximum Input RF Power ..... –20dBm

Electrical Characteristics(4)

Specifications apply for 3.0V < V_{DD} < 3.6V, V_{SS} = 0V, C_{AGC} = 4.7µF, C_{TH} = 0.1µF, f_{RX} = 433.92 MHz, unless otherwise noted. **Bold** values indicate –20°C – T_A –70°C. 1kbps data rate (Manchester encoded), reference oscillator frequency = 13.52127MHz.

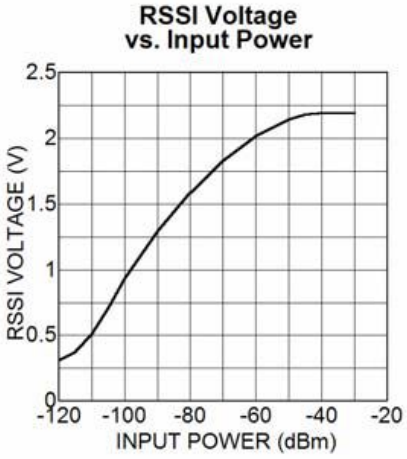
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SS}	Operating Supply Current	Continuous Operation, f_{RX} = 433.92MHz		6.0		mA
I_{SHUT}	Shut down Current			0.5		µA
RF/IF Section						
	Image Rejection			20		dB
	1st IF Center Frequency	f_{RX} = 433.92MHz		1.2		MHz
	Receiver Sensitivity @ 1kbps	f_{RX} = 433.92MHz (matched to 50 Ω) BER=10^{-2}		-110		dBm
	IF Bandwidth	f_{RX} = 433.92MHz		330		kHz
	Antenna Input Impedance	f_{RX} = 433.92MHz		19 – j174		Ω
	Receive Modulation Duty Cycle	Note 5	20		80	%
	AGC Attack / Decay Ratio	t_{ATTACK} / t_{DECAY}		0.1		
	AGC pin leakage current	T_A = 25ºC T_A = +105ºC		± 2 ± 800		nA nA
	AGC Dynamic Range	RF_{IN} @ -40dBm		1.15		V
		RF_{IN} @ -100dBm		1.70		V
Reference Oscillator						
	Reference Oscillator Frequency	f_{RX} = 433.92 MHz Crystal Load Cap = 10pF		13.52127		MHz
	Reference Oscillator Input Impedance			300		kΩ
	Reference Oscillator Input Range		0.2		1.5	Vp-p
	Reference Oscillator Source Current	V(REFOSC) = 0V		3.5		µA

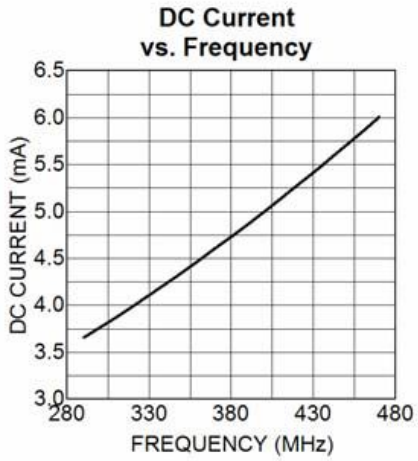
Demodulator						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Units**
	CTH Source Impedance	F_{REFOSC} = 13.52127MHz		120		kΩ
	CTH Leakage Current	T_A = 25ºC T_A = +105ºC		± 2 ± 800		nA nA
	Demodulator Filter Bandwidth @ 434MHz	Programmable, see application section	1625		13000	Hz
Digital / Control Functions						
	DO pin output current	As output source @ 0.8 Vdd sink @ 0.2 Vdd		260 600		µA
	Output rise and fall times	Cl = 15pF, pin DO, 10-90%		2		µsec
RSSI						
	RSSI DC Output Voltage Range			0.4 to 2		V
	RSSI response slope	-110dBm to -40dBm		25		mV/dB
	RSSI Output Current			400		µA
	RSSI Output Impedance			200		Ω
	RSSI Response Time	50% data duty cycle, input power to Antenna = -20dBm		0.3		sec

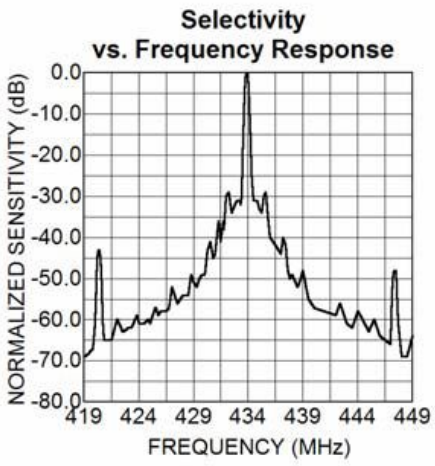
Note 1. Exceeding the absolute maximum rating may damage the device.
Note 2. The device is not guaranteed to function outside of its operating rating.
Note 3. Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.
Note 4. Sensitivity is defined as the average signal level measured at the input necessary to achieve 10-2 BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded) at a data rate of 1kbps.
Note 5. When data burst does not contain preamble, duty cycle is defined as total duty cycle, including any "quiet" time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor C , then duty cycle is the effective duty cycle of the burst alone. [For example, 100msec burst with 50% duty cycle, and 100msec "quiet" time between bursts. If burst includes preamble, duty cycle is T_{ON} /(T_{ON}+T_{OFF})= 50%; without preamble, duty cycle is T_{ON} /(T_{ON}+T_{OFF} + Tquiet) = 50msec/(200msec)=25%. T_{ON} is the (Average number of 1's/burst) × bit time, and T_{OFF}= T_{BURST}– T_{ON}).

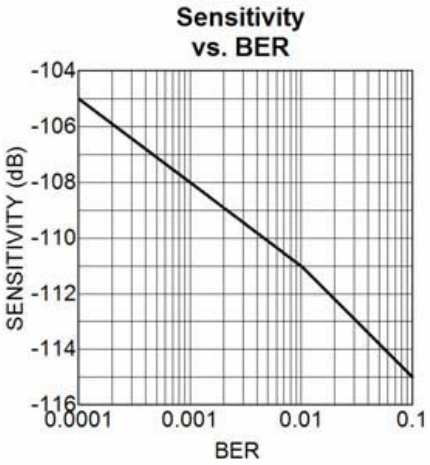
Typical Characteristics

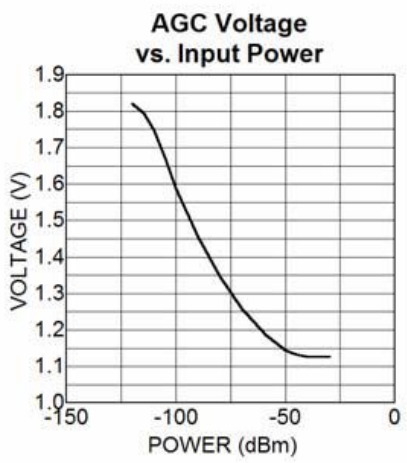
Sensitivity Graphs

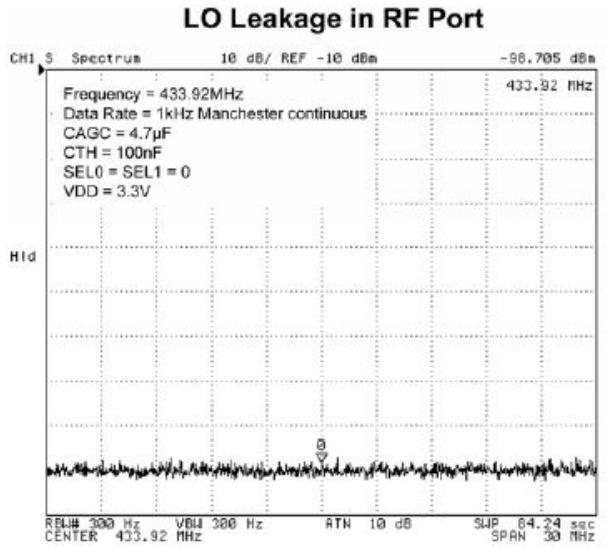












Functional Diagram

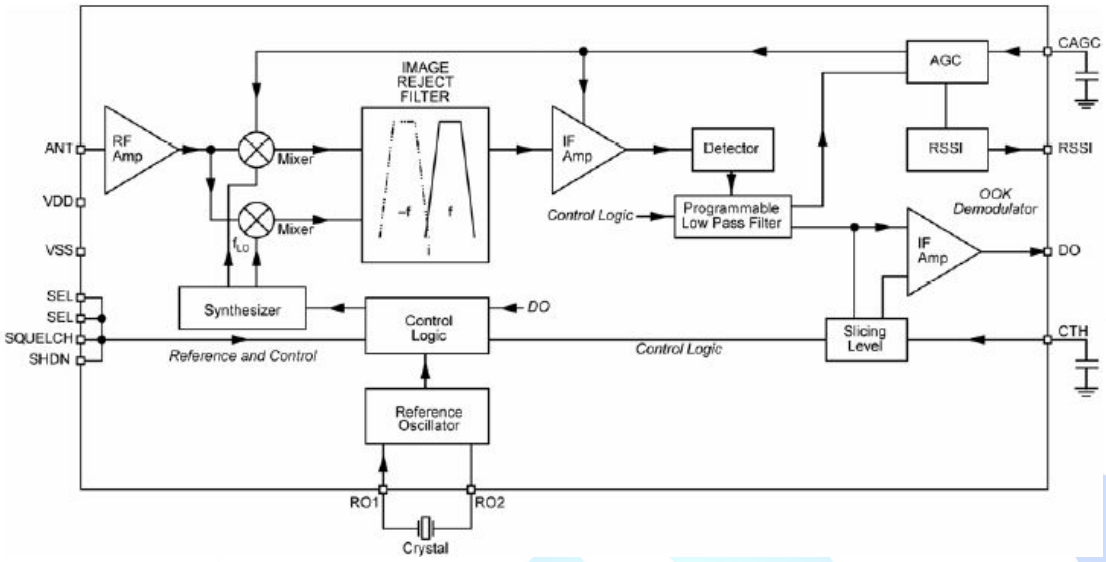


Figure 1, CY803/802 Simplified Block Diagram.

Functional Description

Figure 1. Simplified Block Diagram that illustrates the basic structure of the CY803/802. It is made of three sub-blocks; Image Rejection UHF Down-converter, the OOK Demodulator, and Reference and Control Logics. Outside the device, the CY803/802 requires only three components to operate: two capacitors (CTH, and CAGC) and the reference frequency device, usually a quartz crystal. An additional five components may be used to improve performance. These are: power supply decoupling capacitor, two components for the matching network, and two components for the pre-selector band pass filter.

Receiver Operation

LNA

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA is a Cascoded NMOS.

Mixers and Synthesizer

The LO ports of the Mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal to allow suppression of the image frequency at twice the IF frequency below the wanted signal. The local oscillator is set to 32 times the crystal reference frequency via a phase-locked loop synthesizer with a fully integrated loop filter.

Image Reject Filter and Band-Pass Filter

The IF ports of the mixer produce quadrature down converted IF signals. These IF signals are low-pass filtered to remove higher frequency products prior to the image reject filter where they are combined to reject the image frequencies. The IF signal then passes through a third order band pass filter. The IF center frequency is 1.2MHz. The IF BW is 330kHz @ 433.92MHz, and this varies with RF operating frequency. The IF BW can be calculated via direct scaling:

$$BW_{IF} = BW_{IF@433.92\ MHz} \times \left(\frac{\text{Operating Freq (MHz)}}{433.92} \right)$$

These filters are fully integrated inside the CY803/802. After filtering, four active gain controlled amplifier stages enhance the IF signal to proper level for demodulation.

OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, and AGC comparator.

Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes base band information. The programmable low-pass filter further enhances the base band information. There are four programmable low-pass filter BW settings: 1625Hz, 3250Hz, 6500Hz, 13000Hz for 433.92MHz operation. Low pass filter BW will vary with RF Operating Frequency. Filter BW values can be easily calculated by direct scaling. See equation below for filter BW calculation:

$$BW_{Operating\ Freq} = BW_{@433.92MHz} * \left(\frac{Operating\ Freq\ (MHz)}{433.92}\right)$$

It is very important to choose the filter setting that best fits the intended data rate to minimize data distortion. Demod BW is set at 13000Hz @ 433.92MHz as default (assuming both SEL0 and SEL1 pins are floating). The low pass filter can be hardware set by external pins SEL0 and SEL1.

SEL0	SEL1	Demod BW (@ 434MHz)
0	0	1625Hz
1	0	3250Hz
0	1	6500Hz
1	1	13000Hz - default

Table 1. Demodulation BW Selection

Slicer, Slicing Level and Squelch

The signal prior to slicer is still linear demodulated AM. Data slicer converts this signal into digital "1"s and "0"s by comparing with the threshold voltage built up on the CTH capacitor. This threshold is determined by detecting the positive and negative peaks of the data signal and storing the mean value. Slicing threshold default is 50%. After the slicer the signal is now digital OOK data.

During long periods of "0"s or no data period, threshold voltage on the CTH capacitor may be very low. Large random noise spikes during this time may cause erroneous "1"s at DO pin. Squelch pin when pull down low will suppress these errors.

AGC Comparator

The AGC comparator monitors the signal amplitude from the output of the programmable low-pass filter. When the output signal is less than 750mV thresh-hold, 1.5µA current is sourced into the external CAGC capacitor. When the output signal is greater than 750mV, a 15µA current sink discharges the CAGC capacitor. The voltage developed on the CAGC capacitor acts to adjust the gain of the mixer and the IF amplifier to compensate for RF input signal level variation.

Reference Control

There are 2 components in Reference and Control sub-block: 1) Reference Oscillator and 2) Control Logic through parallel Inputs: SEL0, SEL1, SHDN

Reference Oscillator

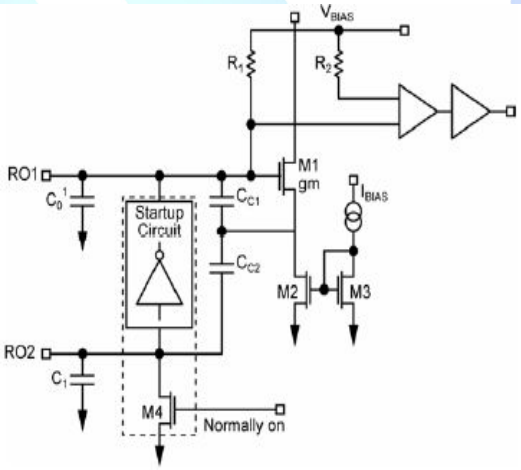


Figure 2: Reference Oscillator Circuit

The reference oscillator in the CY803/802 (Figure 2) uses a basic Colpitts crystal oscillator configuration with MOS transconductor to provide negative resistance. All capacitors shown in Figure 2 are integrated inside CY803/802. R01 and R02 are external pins of CY803/802. User only needs to connect reference oscillation crystal.

Reference oscillator crystal frequency can be calculated:

$F_{REF\ OSC} = F_{RF}/(32 + 1.1/12)$

For 433.92 MHz, $F_{REF\ OSC}$ = 13.52127 MHz.

To operate the CY803/802 with minimum offset, crystal frequencies should be specified with 10pF loading capacitance.

Application Information

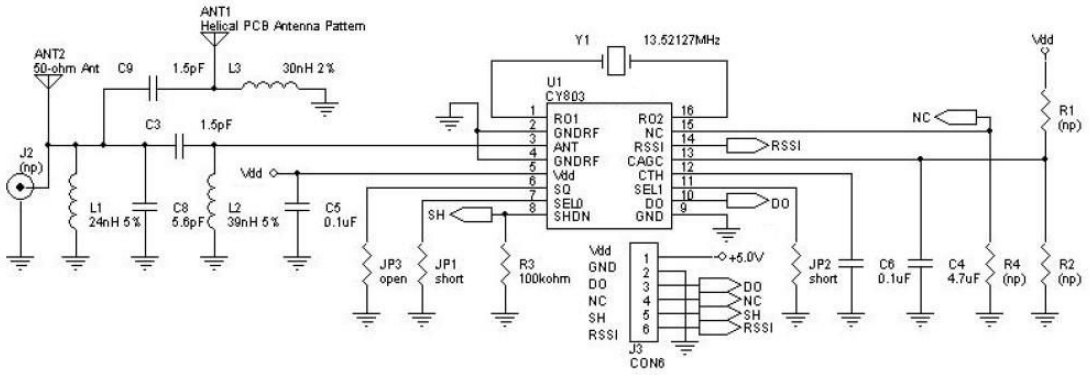


Figure 3. CY803/802 Application Example, 433.92 MHz

The CY803/802 can be fully tested by using one of many evaluation boards designed at CY for this device. As an entry level, the CY803/802 (Figure 3) offers a good start for most applications. It has a helical PCB antenna with its matching network, a band-pass-filter front-end as a pre-selector filter, matching network and the minimum components required to make the device work, which are a crystal, Cagc, and Cth capacitors. By removing the matching network of the helical PCB antenna (C9 and L3), a whip antenna (ANT2) or a RF connector (J2) can be used instead. Figure 3 shows the entire schematic of it for 433.92MHz. Other frequencies can be used and the values needed are in the tables below. Capacitor C9 and inductor L3 are the passive elements for the helical PCB matching network. A tight tolerance is recommended for these devices, like 2% for the inductor and 0.1pF for the capacitor. PCB variations may require different values and optimization. Table 2 shows the matching elements for the device frequency range. For additional information look for Small PCB Antennas for CY RF Products application note.

Freq (MHz)	C9 (pF)	L3(nH)
390.0	1.2	43
418.0	1.2	36
433.92	1.5	30

Table 2. Matching Values for the Helical PCB Antenna

To use another antenna, like the whip kind, remove C9 and place the whip antenna in the hole provided in the PCB. Also, a RF signal can be injected there. L1 and C8 form the pass-band-filter front-end. Its purpose is to attenuate undesired outside band noise which reduces the receiver performance. It is calculated by the parallel resonance equation f = 1/(2×PI×(SQRT L1×C8)). Table 3 shows the most used frequency values.

Freq (MHz)	C8 (pF)	L1(nH)
390.0	6.8	24
418.0	6.0	24
433.92	5.6	24

Table 3. Band-Pass-Filter Front-End Values

There is no need for the band-pass-filter front-end for applications where it is proven that the outside band noise does not cause a problem. The CY803/802 has image reject mixers which improve significantly the selectivity and rejection of outside band noise.

Capacitor C3 and inductor L2 form the L-shape matching network. The capacitor provides additional attenuation for low frequency outside band noise and the inductor provides additional ESD protection for the antenna pin. Two methods can be used to find these values, which are matched close to 50Ω. One method is done by calculating the values using the equations below and another by using a Smith chart. The latter is made easier by using software that plots the values of the components C8 and L1, like WinSmith by Noble Publishing.

To calculate the matching values, one needs to

know the input impedance of the device. Table 4 shows the input impedance of the CY803/802 and suggested matching values for the most used frequencies. These suggested values may be different if the layout is not exactly the same as the one made here.

Freq (MHz)	C3 (pF)	L2(nH)	Z device (Ω)
390.0	1.5	47	22.5 – j198.5
418.0	1.5	43	21.4 – j186.1
433.92	1.5	39	18.6 – j174.2

Table 4: matching values for the most used frequencies For the frequency of 433.92MHz, the input impedance is Z = 18.6 – j174.2Ω, then the matching components are calculated by,

Equivalent parallel = B = 1/Z = 0.606 + j5.68 msiemens

Rp = 1 / Re (B); Xp = 1 / Im (B)

Rp = 1.65kΩ; Xp = 176.2Ω

Q = SQRT (Rp/50 + 1)

Q = 5.831

Xm = Rp / Q

Xm = 282.98Ω

Resonance Method For L-shape Matching Network

Lc = Xp / (2×Pi×f); Lp = Xm / (2×Pi×f)

L2 = (Lc×Lp) / (Lc + Lp); C3 = 1 / (2×Pi×f×Xm)

L2 = 39.8nH

C3 = 1.3pF

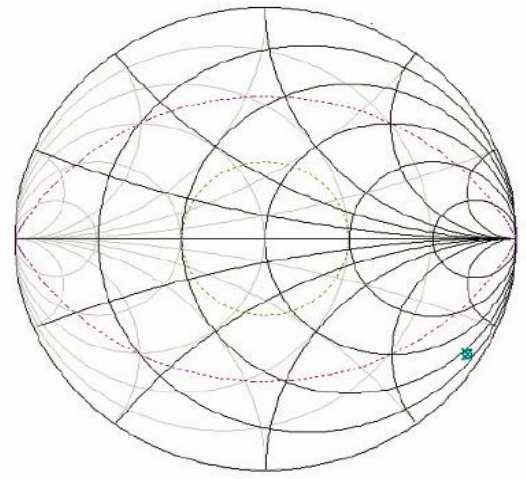


Figure 4: device's input impedance, Z = 18.6 – j174.2Ω

Doing the same calculation example with the Smith Chart, it would appear as follows,

Figure 4: device's input impedance, Z = 18.6 – j174.2Ω

First, we plot the input impedance of the device, (Z = 18.6 – j174.2)Ω @ 433.92MHz (Figure 4). Second, we plot the shunt inductor (39nH) and the series capacitor (1.5pF) for the desired input impedance (Figure 5). We can see the matching leading to the center of the Smith Chart or close to 50Ω.

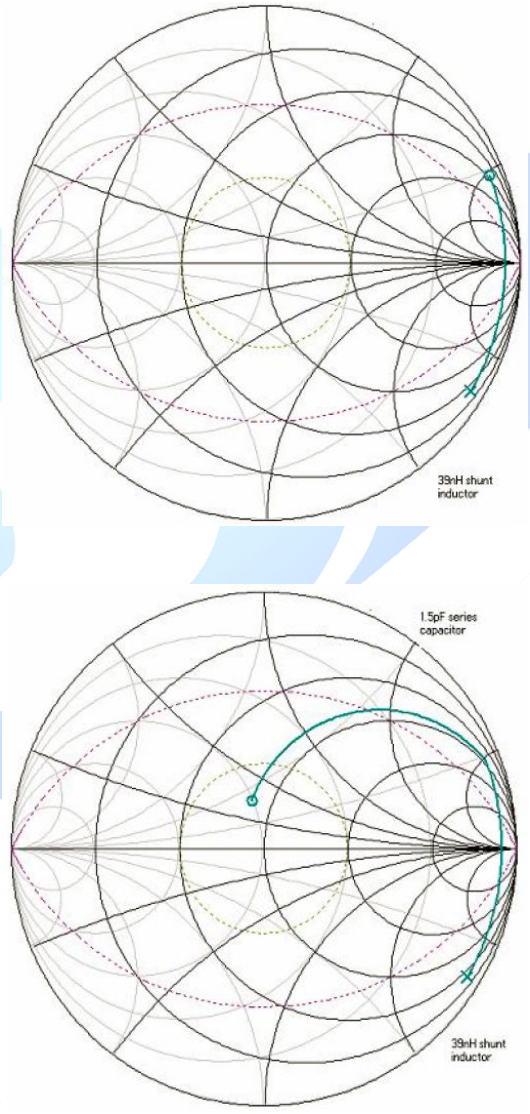


Figure 5. Plotting the Shunt Inductor and Series Capacitor

Crystal Y1 or Y1A (SMT or leaded respectively) is the reference clock for all the device internal circuits. Crystal characteristics of 10pF load capacitance, 20ppm, ESR < 50Ω, -20°C to

+70ºC temperature range are desired. Table 5 shows the crystal frequencies and one of CY company approved crystal manufacturers. The oscillator of the CY803/802 is a Colpitts type. It is very sensitive to stray capacitance loads. Thus, very good care must be taken when laying out the printed circuit board. Avoid long traces and ground plane on the top layer close to the REFOSC pins RO1 and RO2. When care is not taken in the layout, and crystals from other vendors are used, the oscillator may take longer times to start as well as the time to good data in the DO pin to show up. In some cases, if the stray capacitance is too high (> 20pF), the oscillator may not start at all.

The crystal frequency is calculated by REFOSC = RFCarrier/(32+(1.1/12)). The local oscillator is low side injection (32 × 13.52127MHz = 432.68MHz), that is, its frequency is below the RF carrier frequency and the image frequency is below the LO frequency. See Figure 6. The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which will be demodulated by the detector of the device.

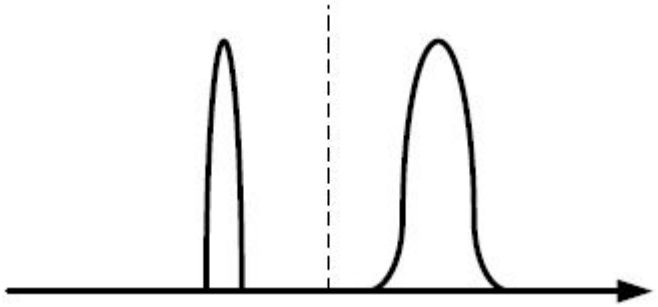


Figure 6. Low Side Injection Local Oscillator.

REFOSC (MHz)	Carrier (MHz)	CY Part Number
12.15269	390.0	S-12.15269M
13.02519	418.0	S-13.02519M
13.52127	433.92	S-13.52127M

Table 5. Crystal Frequency and Vendor Part Number.

JP1 and JP2 are the bandwidth selection for the demodulator bandwidth. To set it correctly, it is necessary to know the shortest pulse width of the encoded data sent in the transmitter. Like in the example of the data profile in the figure 7 below, PW2 is shorter than PW1, so PW2 should be used for the demodulator bandwidth calculation which is found by 0.65/shortest pulse width. After this value is found, the setting should be done according to Table 6. For example, if the pulse period is 100µsec, 50% duty cycle, the pulse width will be 50µsec (PW = (100µsec × 50%) / 100). So, a bandwidth of 13kHz would be necessary (0.65 / 50µsec). However, if this data stream had a pulse period with 20% duty cycle, the bandwidth required would be 32.5kHz (0.65 / 20µsec), which exceeds the maximum bandwidth of the demodulator circuit. If one tries to exceed the maximum bandwidth, the pulse would appear stretched or wider. Other frequencies will have different demodulator bandwidth limits, which are derived from the reference oscillator frequency. Table 7 and Table 8 below shows the limits for the other two most used frequencies.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (hertz)
Short	Short	1625	400	1250
Open	Short	3250	200	2500
Short	Open	6500	100	5000
Open	Open	13000	50	10000

Table 6. JP1 and JP2 setting, 433.92 MHz.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (hertz)
Short	Short	1565	416	1204
Open	Short	3130	208	2408
Short	Open	6261	104	4816
Open	Open	12523	52	9633

Table 7. JP1 and JP2 setting, 418.0 MHz.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (Hertz)
Short	Short	1460	445	1123
Open	Short	2921	223	2246
Short	Open	5842	111	4493
Open	Open	11684	56	8987

Table 8. JP1 and JP2 setting, 390.0 MHz.

Capacitors C6 and C4, CTH and CAGC respectively provide time base reference for the data pattern received. These capacitors are selected according to data profile, pulse duty cycle, dead time between two received data packets, and if the data pattern has or does not have a preamble. See Figure 7, example of a data profile.



Figure 7. Example of a Data Profile.

For best results the capacitors should always be optimized for the data pattern used. As the baud rate increases, the capacitor values decrease. Table 9 shows suggested values for Manchester Encoded data, 50% duty cycle.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Cth	Cagc
Short	Short	1625	100nF	4.7µF
Open	Short	3250	47nF	2.2µF
Short	Open	6500	22nF	1µF
Open	Open	13000	10nF	0.47µF

Table 9. Suggested CTH and CAGC Values.

JP3 is a jumper used to configure the digital squelch function. When it is high, there is no squelch applied to the digital circuits and the DO (data out) pin has a hash signal. When the pin is low, the DO pin activity is considerably reduced. It will have more or less than shown in the figure below depending on the outside band noise. The penalty for using squelch is a delay in getting a good signal in the DO pin, that is, it takes longer for the data to show up. The delay is dependent upon many factors such as RF signal intensity, data profile, data rate, CTH and CAGC capacitor values, and outside band noise. See Figure 8 and Figure 9 below.

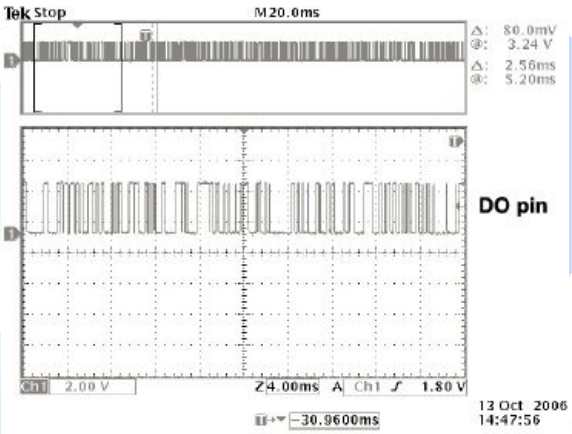


Figure 8. Data Out Pin with No Squelch (SQ = 1).

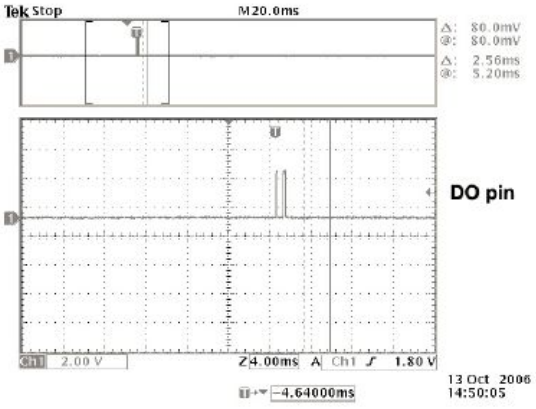


Figure 9. Data Out Pin with Squelch (SQ = 0).

Other components used are C5, which is a decoupling capacitor for the Vdd line, R4 reserved for future use and not needed for the evaluation board, R3 for the shutdown pin (SHDN = 0, device is operation), which can be removed if that pin is connected to a microcontroller or an external switch, R1 and R2

which form a voltage divider for the AGC pin. One can force a voltage in this AGC pin to purposely decrease the device sensitivity. Special care is needed when doing this operation, as an external control of the AGC voltage may vary from lot to lot and may not work the same for several devices.

Three other pins are worthy of comment. They are the DO, RSSI, and shut down pin. The DO pin has a driving capability of 0.4mA. This is good enough for most of the logic family ICs in the market today. The RSSI pin provides a transfer function of the RF signal intensity vs voltage. It is very useful to determine the signal to noise ratio of the RF link, crude range estimate from the transmitter source and AM demodulation, which requires a low C_{AGC} capacitor value.

The shut down pin (SHDN) is useful to save energy. When its level close to V_{DD} (SHDN = 1), the device is not in operation. Its DC current consumption is less than 1µA (do not forget to remove R3). When toggling from high to low, there will be a time required for the device to come to steady state mode, and a time for data to show up in the DO pin. This time will be dependent upon many things such as temperature, crystal used, and if the there is an external oscillator with faster startup time. Normally, with the crystal vendors suggested, the data will show up in the DO pin around 1msec time, and 2msec over the temperature range of the device. When using an external oscillator or reference oscillator signal, the time is reduced considerably and can be around 140µsec. See Figures Figure 10 and 11.

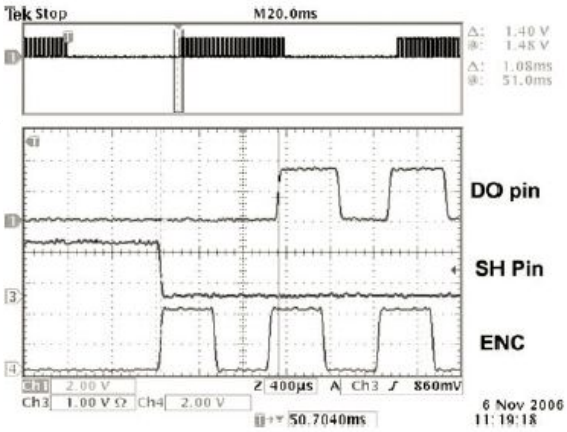


Figure 10: Time-to-Good Data After Shut Down Cycle, Room Temperature.

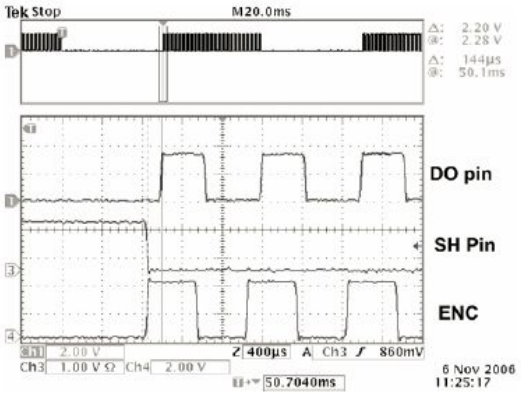
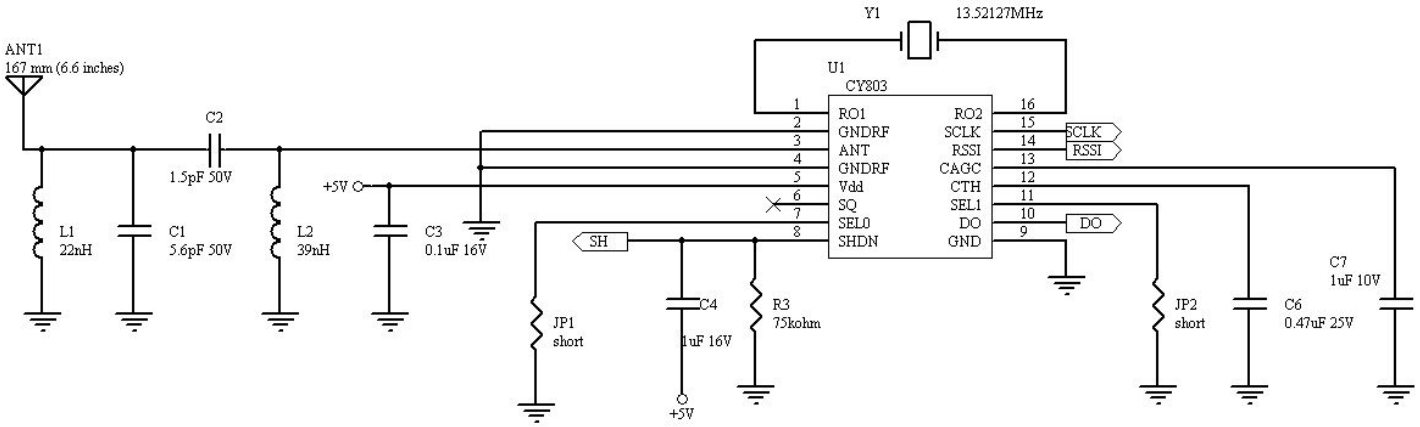


Figure 11. Time to Good Data, External Oscillator, Room Temperature.

Figure1 CY803/802 Receiver 433.92MHz Module



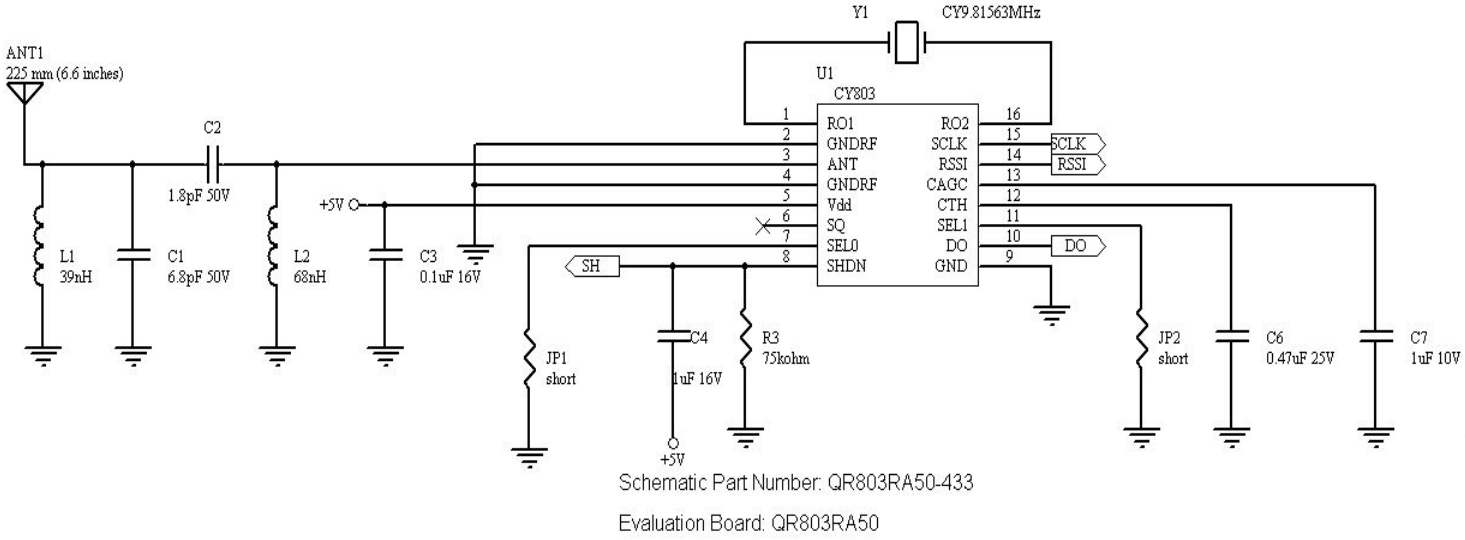
Schematic Part Number: QR803RA50-433

Evaluation Board: QR803RA50

CY803/802 Bill of Materials, 433.92 MHz

Item	Manufacturer	Description	Qty.
C1	MuRata	5.6pF , 0402/0603	1
C2	MuRata	1.5pF , 0402/0603	1
C3	MuRata	0.1uF , 0402/0603	1
C4	MuRata	1uF , 0402/0603	1
C6	MuRata	0.47uF , 0402/0603	1
C7	MuRata	1uF, 0402/0603	1
JP1		short	1
JP2		short	1
R3		75Kohm	1
L1	MuRata	22nH 5%, 0402/0603	1
L2	MuRata	39nH 5%, 0402/0603	1
U1	CY803/802	SSOP-16/SOP-16	1
Y1	CY13.52127MHz	HC49S	1

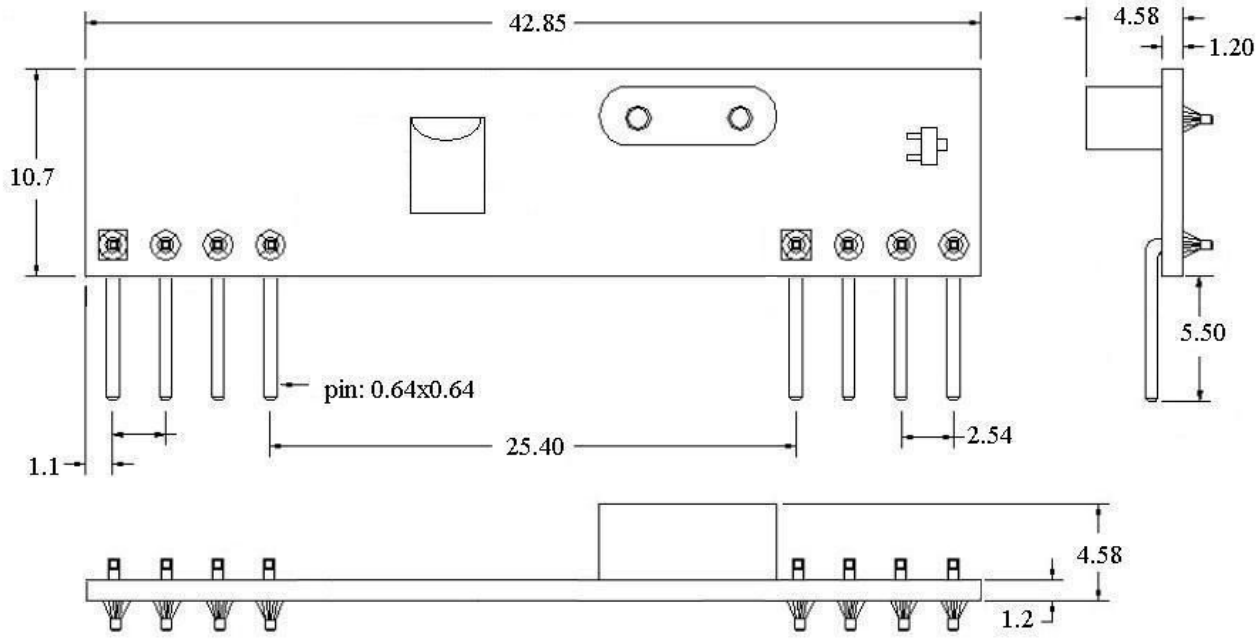
Figure1 CY803/802 Receiver 315MHz Module



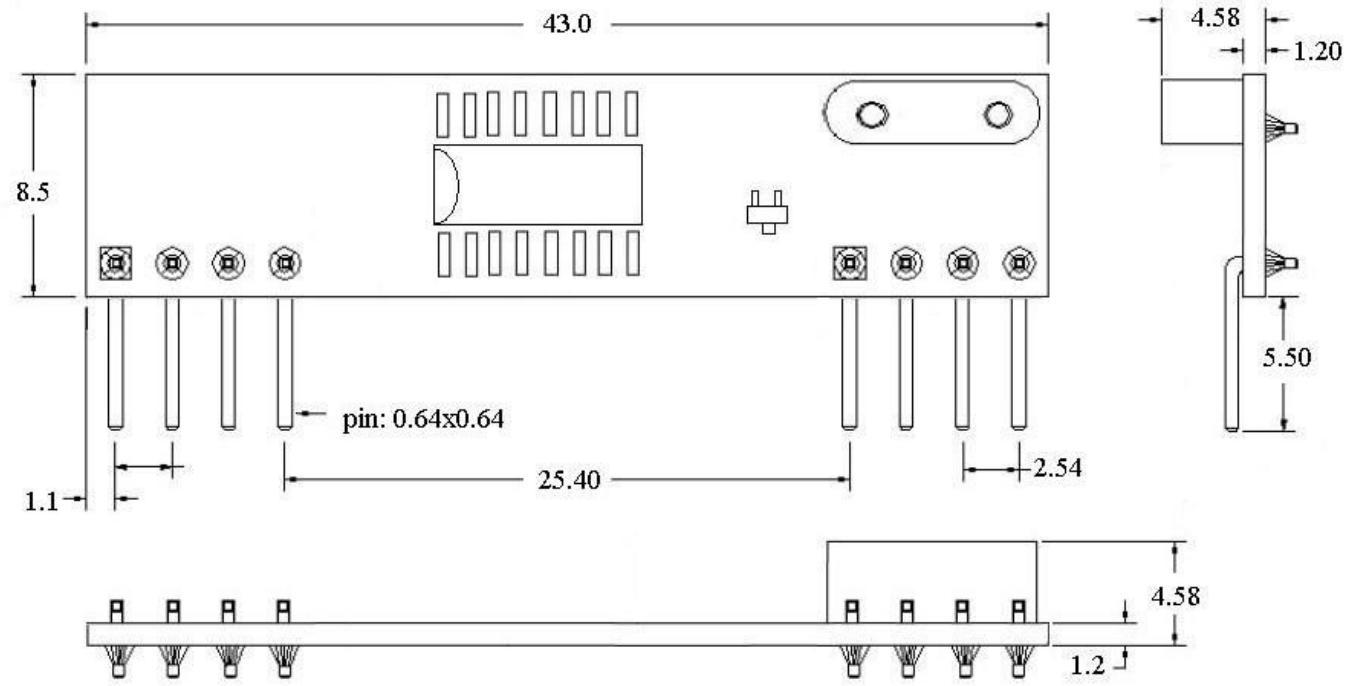
CY803/802 Bill of Materials, 315 MHz

Item	Manufacturer	Description	Qty.
C1	MuRata	6.8pF , 0402/0603	1
C2	MuRata	1.8pF , 0402/0603	1
C3	MuRata	0.1uF , 0402/0603	1
C4	MuRata	1uF , 0402/0603	1
C6	MuRata	0.47uF , 0402/0603	1
C7	MuRata	1uF, 0402/0603	1
JP1		short	1
JP2		short	1
R3		75Kohm	1
L1	MuRata	39nH 5%, 0402/0603	1
L2	MuRata	68nH 5%, 0402/0603	1
U1	CY803/802	SSOP-16/SOP-16	1
Y1	CY9.81563MHz	HC49S	1

CY803/802 Module Mechanical Size: (unit: mm)



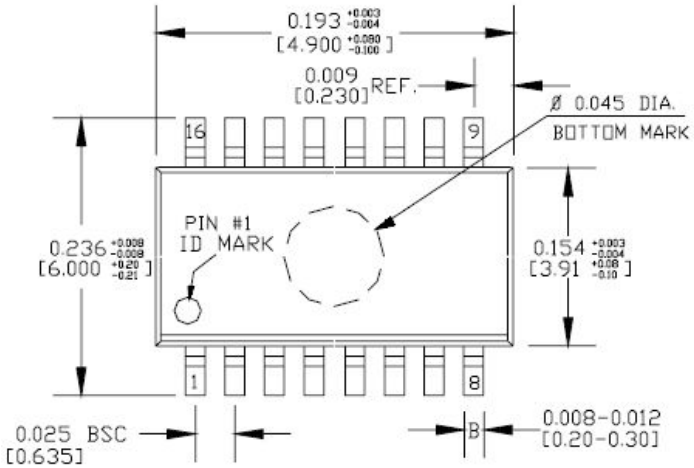
SSOP16 Module Shape

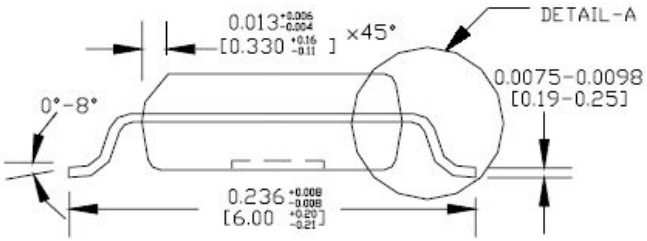


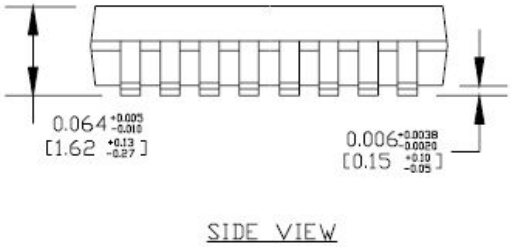
SOP16 Module Shape

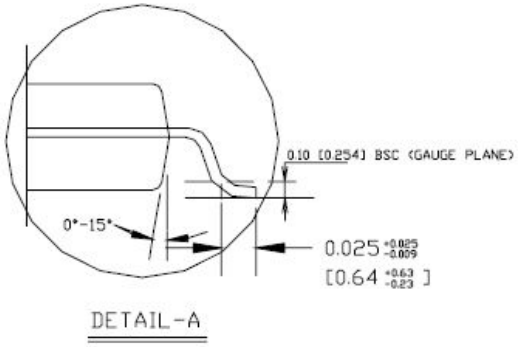
Package Information: (unit: mm)

SSOP16 Package

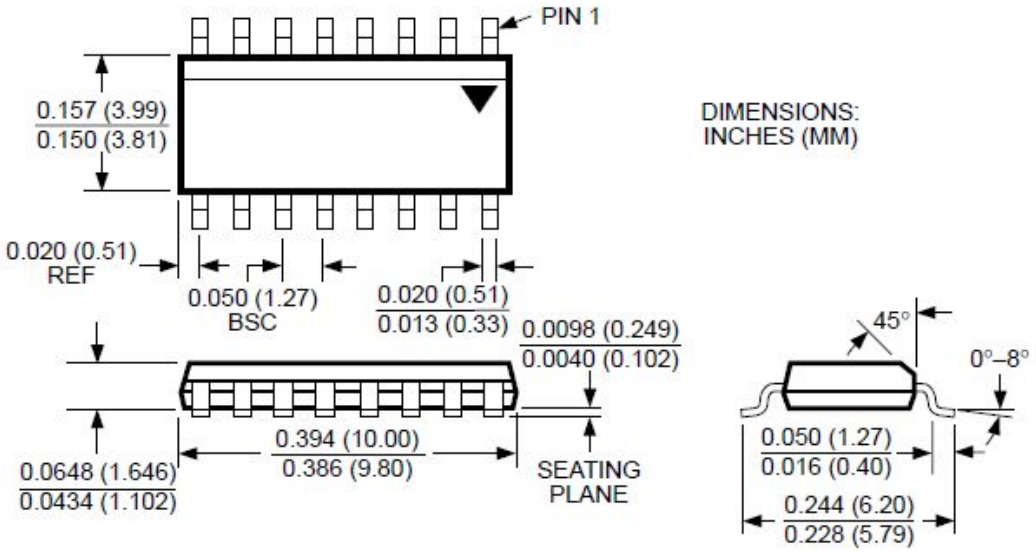




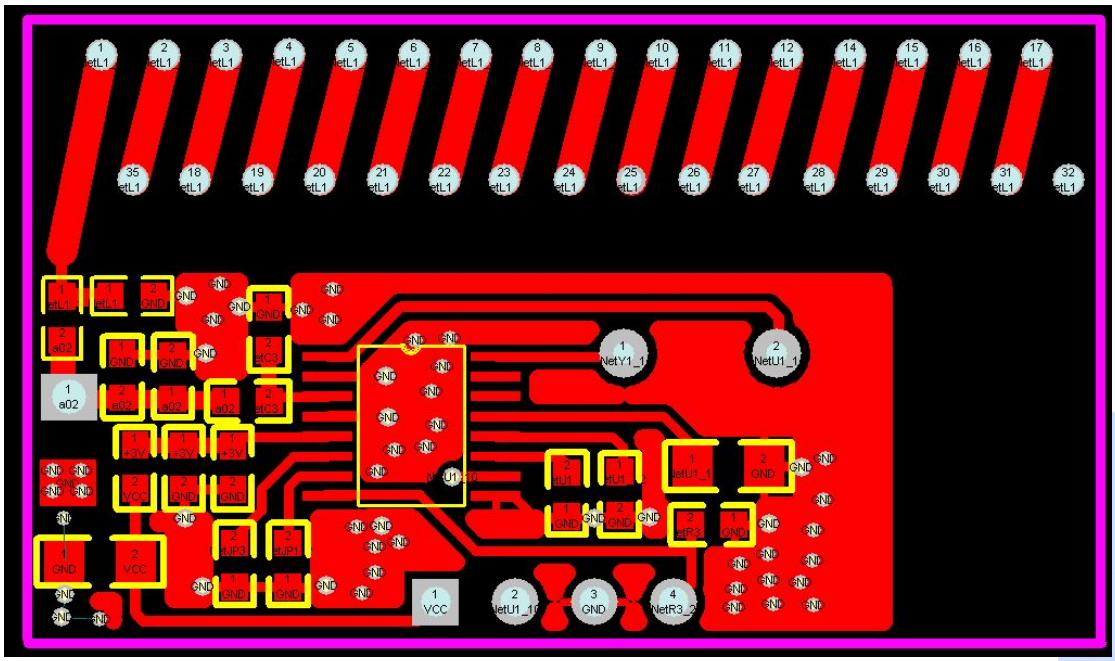


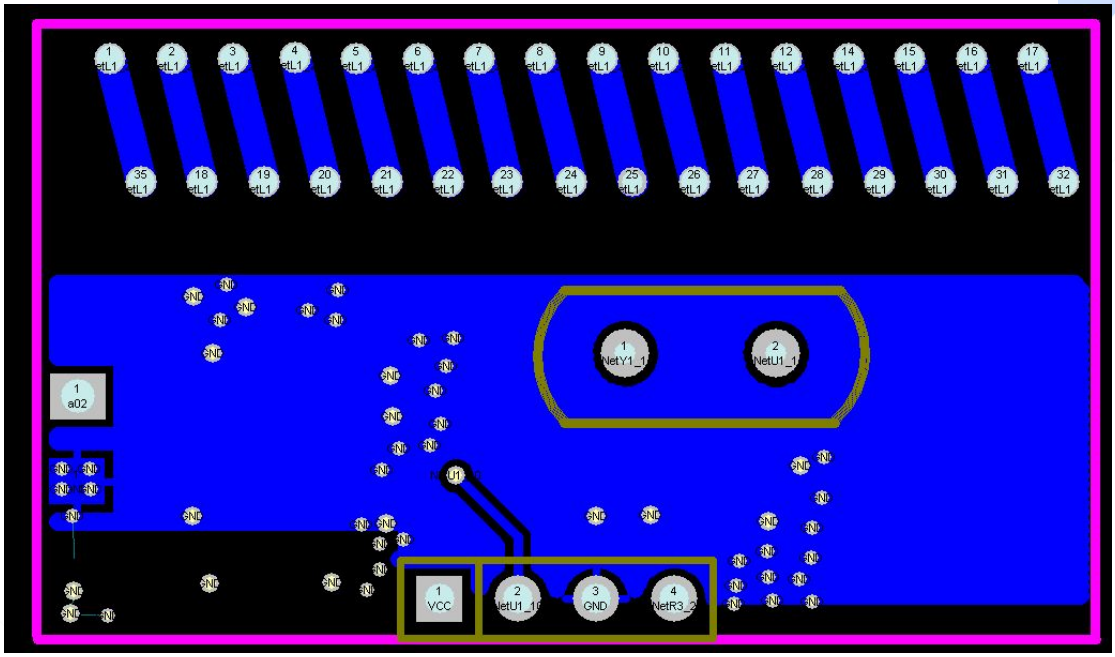


SOP16 Package



CY803/802 PCB antenna：





For more information and assistance, please contact us as follows:

CY WIRELESS TECHNOLOGY LIMITED

Website：www.rficy.com

Email: info@rficy.com