CY800/801 Datasheet

300M-450MHz RF receiver

General Description

The CY800/801 is a single chip ASK/OOK (ON-OFF Keyed) RF receiver IC. This device is a true "antenna-in to data-out" monolithic device. All RF and IF tuning are accomplished automatically within its side, which eliminates manual tuning and reduces production cost. All IF filtering and post-detection (demodulator) data filtering is provided within the IC side, so no external filters are necessary. One of four demodulator filter bandwidths may be selected externally by the user. The result is a highly reliable yet low cost solution. The device with a set of easily determined values, based upon data rate, code modulation format, and desired duty-cycle operation.

The CY801 offer two modes of operation: fixed-mode (FIX) and sweep-mode (SWP), CY800 only work in fixed-mode (FIX). In fixed mode its function as a conventional super-heterodyne receiver. In sweep mode the CY801 sweeps a wider RF spectrum. Fixed-mode provides better selectivity and sensitivity performance and sweep mode enables the CY801 to be used with low cost, imprecise transmitters.

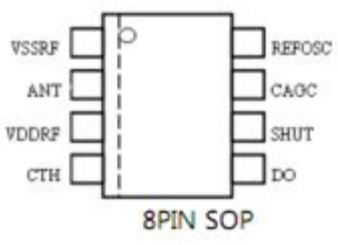
Features

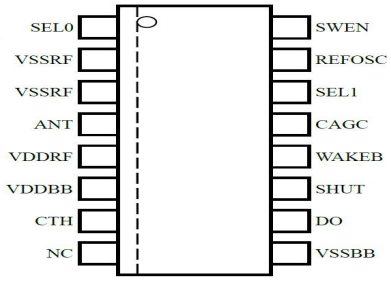
- Frequency from 300MHz to 440MHz
- Voltage: 3.3V-5.5V
- Sensitivity: –106 dBm sensitivity, 1kbps and BER 10E-02
- Data-rate up to 8kbps (fixed-mode)
- Low Power Consumption
  - ■ 2.7mA fully operational (315MHz) 3.7mA fully operational (433MHz)
  - ■ 0.9μA in shutdown
  - ■250μA in polled operation (10:1 duty-cycle)
- Very low RF re-radiation at the antenna
- Highly integrated with extremely low external part count

Ordering Information

Ordering Info Part Number	Temperature Range	Package
CY800	–40° to +85°C	8-Pin SOP
CY801	–40° to +85°C	16-Pin SOP

Pin Configuration:





CY800 Pins **CY801 Pins（SOP16）**

Pin Description

Pin Number 16-Pin Pkg.		Pin Name	Pin Function
1		SEL0	Bandwidth Selection Bit 0 (Digital Input): Used in conjunction with SEL1 to set the desired demodulator filter bandwidth. See Table 1. Internally pulled-up to VDDRF
2, 3		VSSRF	RF Power Supply: Ground return to the RF section power supply.
4		ANT	Antenna (Analog Input): For optimal performance the ANT pin should be impedance matched to the antenna. See "Applications Information" for information on input impedance and matching techniques
5		VDDRF	RF Power Supply: Positive supply input for the RF section of the IC
6		VDDBB	Base-Band Power Supply: Positive supply input for the baseband section (digital section) of the IC
7		CTH	Data Slicing Threshold Capacitor (Analog I/O): Capacitor connected to this pin extracts the dc average value from the demodulated waveform which becomes the reference for the internal data slicing comparator
8		NC	Not internally connected
9		VSSBB	Base-Band Power Supply: Ground return to the baseband section power supply
10		DO	Data Output (Digital Output)
11		SHUT	Shutdown (Digital Input): Shutdown-mode logic-level control input. Pull low to enable the receiver. Internally pulled-up to VDDRF
12		WAKEB	Wakeup (Digital Output): Active-low output that indicates detection of an incoming RF signal
13		CAGC	Automatic Gain Control (Analog I/O): Connect an external capacitor to set the attack/decay rate of the on-chip automatic gain control
14		SEL1	Bandwidth Selection Bit 1 (Digital Input): Used in conjunction with SEL0 to set the desired demodulator filter bandwidth. See Table 1. Internally pulled-up to VDDRF
15		REFOSC	Reference Oscillator: Timing reference, sets the RF receive frequency.
16		SWEN	Sweep-Mode Enable (Digital Input): Sweep- or Fixed-mode operation control input. SWEN high= sweep mode; SWEN low = conventional superheterodyne receiver. Internally pulled-up to VDDRF

AbsoluteMaximum Ratings(1)

Supply Voltage (VDD).....+5.5V
Input Voltage..... ..... +5V
Junction temperature..... ... +150ºC
Lead Temperature (soldering, 10sec.) .... 260°C
Storage Temperature (TS).....-65ºC to +150°C
ESD Rating(3) .....2KV CDM

Operating Ratings(2)

Supply voltage (V_{DD}).....+3.3V to +5.5V
Ambient Temperature (T_A).... –40°C to +85°C
Input Voltage (V_{IN})..... 5.5V (Max)

Electrical Characteristics

Specifications apply for $V_{DDRF}=V_{DDBB}=V_{DD}$, $+4.75 \le V_{DD} \le 5V$, $V_{SS}=0V$; $C_{AGC}=4.7uF$, $C_{TH}=100nF$; SEL0=SEL1=VSS; fixed mode(SWEN= V_{SS}); $F_{REFOSC}=4.8970MHz$（i.e. $f_{RF}=315MHz$）; baud rate=1kbps(Manchester encoded); bold values indicate –40 C ≤ TA ≤ +85 C; unless otherwise n o t e d .

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OP}	Operating Current	continuous operation, f_{RF} = 315MHz		2.5	3.5	mA
		polled with 10:1 duty cycle, f_{RF} = 315MHz		300		uA
		continuous operation, f_{RF} = 433.92MHz		3	4	mA
		polled with 10:1 duty cycle, f_{RF} = 433.92MHz		500		uA
I_{STBY}	Standby Current	$V_{SHUT} = V_{DD}$		0.9		uA

RF Section, IF Section

	Receiver Sensitivity (Note 4)	f_{RF} = 315MHz		–108		dBm
		f_{RF} = 433.92MHz		–107		dBm
f_{IF}	IF	Center		0.86		MHz
f_{BW}	IF	Bandwidth		0.43		MHz
	Maximum Receiver Input	R_{SC} = 50Ω		-20		dBm
	Spurious Reverse Isolation	ANT pin, R_{SC} = 50Ω, Note 5		30		uVrms
	AGC Attack to Decay Ratio	$t_{ATTACK} \div t_{DECAY}$		0.1		
	AGC Leakage Current	T_A = +85°C		±100		nA

Reference Oscillator

Z_{REFOSC}	Reference Oscillator Input Impedance				290	kΩ
	Reference Oscillator Source Current				5.2	uA

Demodulator

ZCTH	CTH Source Impedance			145		kΩ
IZCTH(leak)	CTH Leakage Current	TA=+85		± 100		nA
	Demodulator Filter Bandwidth	VSEL0=VDD VSEL1=VDD		4000		Hz
	Sweep Mode	VSEL0=Vss VSEL1=VDD		2000		Hz
	(SWEN = V_{DD} or OPEN)	VSEL0=VDD VSEL1=Vss		1000		Hz

	Note 6	VSEL0=Vss VSEL1=Vss		500		Hz
	Demodulator Filter Bandwidth	VSEL0=VDD VSEL1=VDD		8000		Hz
	Fixed Mode	VSEL0=Vss VSEL1=VDD		4000		Hz
	(SWEN = VSS) Note 6	VSEL0=VDD VSEL1=Vss		2000		Hz
		VSEL0=Vss VSEL1=Vss		1000		Hz

Digital/Control Section

$V_{IN(high)}$	Input-High Voltage	SEL0, SEL1, SWEN			0.8	VDD
$V_{IN(low)}$	Input-Low Voltage	SEL0, SEL1, SWEN	0.2			VDD
I_{OUT}	Output Current	DO, WAKEB pins, push-pull		10		uA
$V_{OUT(high)}$	Output High Voltage	DO, WAKEB pins, I_{OUT} = –1µA	0.9			VDD
$V_{OUT(low)}$	Output Low Voltage	DO, WAKEB pins, I_{OUT} = +1µA			0.1	VDD
t_R, t_F	Output Rise and Fall Times	DO, WAKEB pins, C_{LOAD} = 15pF		10		us

Note 1. Exceeding the absolute maximum rating may damage the device.
Note 2. The device is not guaranteed to function outside its operating rating.
Note 3. Devices are ESD sensitive. Use appropriate ESD precautions. Meets class 1 ESD test requirements, (human body model HBM), in accordance
with MIL-STD-883C, method 3015. Do not operate or store near strong electrostatic fields.
Note 4: Sensitivity is defined as the average signal level measured at the input necessary to achieve 10-2 BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded data) at a data rate of 300b/s. The RF input is assumed to be matched into 50 Ω.
Note 5: Spurious reverse isolation represents the spurious components which appear on the RF input pin (ANT) measured into 50 Ω . with an input RF matching network.
Note 6: Parameter scales linearly with reference oscillator frequency fT. For any reference oscillator frequency other than 4.8970MHz, compute new parameter value as the ratio:

$$\frac{f_{REFOSC}MHz}{4}.8970MHz \times (4.8970MHzIIII)$$

Note 7: Parameter scales inversely with reference oscillator frequency fT. For any reference oscillator frequency other than 4.90MHz, compute new parameter value as the ratio:

$$\frac{4.8970MHz}{f_{REFOSC}MHz} \times (4.8970MHzIIII)$$

Functional Diagram

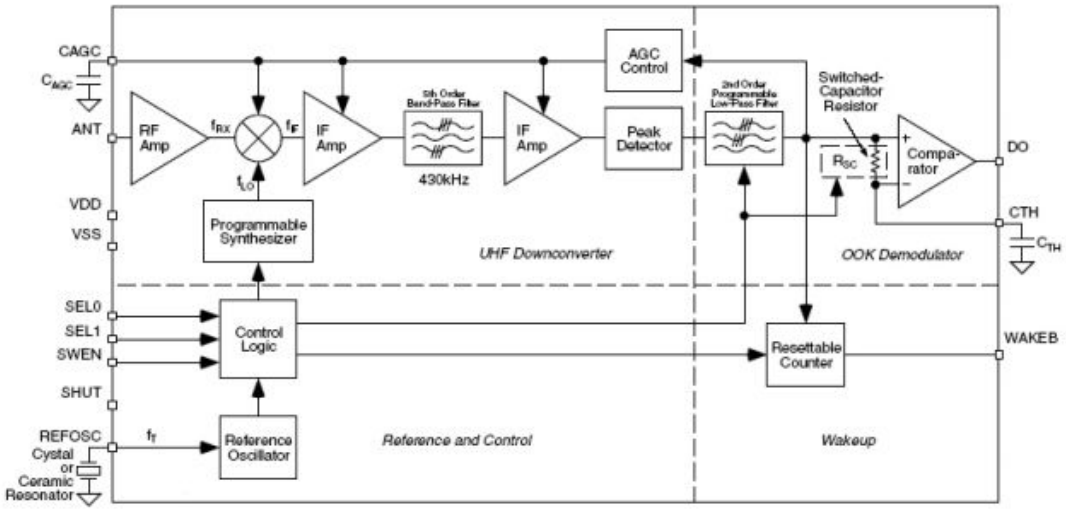


Figure 1, CY801 Simplified Block Diagram.

Functional Description

Refer to Figure1 “CY801 Block Diagram”. Identified in the block diagram are the four sections of the IC: UHF Down-converter, OOK Demodulator, Reference and Control, and Wakeup. Also shown in the figure are two capacitors (CTH, CAGC) and one timing component (Y1), usually a crystal. With the exception of a supply decoupling capacitor, these are the only external components needed by the CY801 to assemble a complete UHF receiver. There is one control input, the SHUT pin. The SHUT function is used to enable the receiver. These inputs are CMOS compatible, and are pulled-up on the IC.

Receiver Operation

The CY801 is a standard super-heterodyne receiver with a narrow RF bandwidth IF. The narrow bandwidth receiver is less susceptible to interfering RF signals. The CY801 is capable of data rates up to 2.1kbps. Typically a crystal is used for the reference oscillator frequency. The CY801RF center frequency is controlled by a completely integrated PLL / VCO frequency synthesizer which is referenced to the crystal frequency. Since the CY801 bandwidth is 430kHz, a tight tolerance transmitter must be used for the system. Typically SAW or crystal based transmitters are used in application designs.

IF Bandpass Filter

Rolloff response of the IF Filter is 5th order, while the demodulator data filter exhibits a 2nd order response.

Baseband Demodulator Filter Bandwidth

The CY801 has a fully integrated baseband demodulator filter. The filter has a fixed 2.1kHz bandwidth. This filter limits the receiver raw data rate to 2kbps.

Data Slicing Level

Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor CTH and the on-chip switched capacitor “resistor” RSC, shown in the block diagram. The effective resistance of RSC is 118kΩ.

Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typically values range from 5ms to 50ms. Optimization of the value of CTH is

required to maximize range.

Automatic Gain Control

The signal path has AGC (automatic gain control) to increase input dynamic range. An external capacitor, C_{AGC}, must be connected to the CAGC pin of the device. The ratio of decay-to-attack time-constant is fixed at 10:1 (that is, the attack time constant is 1/10th of the decay time constant), and this ratio cannot be changed by the user. However, the attack time constant is set externally by choosing a value for C_{AGC}. The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the CY801 in excess of 10:1. When the device is placed into shutdown mode (SHUT pin pulled high), the AGC capacitor floats, to retain the voltage. When operation is resumed, only the voltage droop on the capacitor due to leakage must be replenished, therefore a relatively low-leakage capacitor is recommended for duty-cycled operation. The actual tolerable leakage will be application dependent. Clearly, leakage performance is less critical when the device off-time is low (milliseconds) and more critical when the off-time is high (seconds). To further enhance duty-cycled operation of the IC, the AGC push and pull currents are increased for a fixed time immediately after the device is taken out of shutdown mode (turned on). This compensates for AGC capacitor voltage droop while the IC is in shutdown mode, reduces the time to restore the correct AGC voltage, and therefore extends maximum achievable duty ratios. Push-pull currents are increased by 45 times their nominal values. The fixed time period is based on the reference oscillator frequency f_T, 10.9ms for f_T = 6.00MHz, and varies inversely as f_T varies.

Reference Oscillator

All timing and tuning operations on the CY801 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of two ways:

1. Connect a crystal
2. Drive this pin with an external timing signal

The multiplication factor between the reference oscillator frequency f_T and the internal local oscillator (LO) is 64.5 ~ . For $f_T = f_{LO}$ = 6.00MHz. 64.5 = 387MHz.

The second approach is attractive for lowering system cost further if an accurate reference signal exists elsewhere in the system, for example, a reference clock from a crystal-controlled microprocessor. An externally applied signal should be ac-coupled and resistively-attenuated, or otherwise limited, to approximately 0.5Vpp. The specific reference frequency required is related to the system transmit frequency.

Shutdown Function

The shutdown function is controlled by a logic state applied to the SHUT pin. When V_{SHUT} is high, the device goes into low-power standby mode, consuming less than 1 A. This pin is pulled high internally. It must be externally pulled low to enable the receiver.

Application Steps

The following steps are the basic design steps for using the CY801 receiver:

1) Select the operating mode(sweep or fixed)
2) Select the reference oscillator
3) Select the CTH capacitor
4) Select the CAGC capacitor
5) Select the demodulator filter bandwidth

Step A: Selecting the Operating Mode

A.1 Fixed-Mode Operation

For applications where the transmit frequency is accurately set (that is, applications where a SAW or crystal-based transmitter is used) the CY801 may be configured as a standard super-heterodyne receiver (fixed mode). In fixed-mode operation the RF bandwidth is narrower making the receiver less susceptible to interfering signals. Fixed mode is selected by connecting SWEN to ground.

A.2 Sweep-Mode Operation

When used in conjunction with low-cost L-C transmitters the CY801 should be configured in sweep-mode. In sweep-mode, while the topology is still super-heterodyne, the LO (local oscillator) is swept over a range of frequencies at rates greater than the data rate. This technique effectively increases the RF bandwidth of the CY801, allowing the device to operate in applications where significant transmitter-receiver frequency misalignment may exist. The transmit frequency may vary up to ±0.5% over initial tolerance, aging, and temperature. In sweep-mode a band approximately 1.5% around the nominal transmit frequency is captured. The transmitter may drift CY801 up to ±0.5% without the need to retune the receiver and without impacting system performance. The swept-LO technique does not affect the IF bandwidth, therefore noise performance is not degraded relative to fixed mode. The IF bandwidth is 430kHz whether the device is operating in fixed or sweep-mode. Due to limitations imposed by the LO sweeping process, the upper limit on data rate in sweep mode is approximately 5.0kbps. Similar performance is not currently available with crystal-based super-heterodyne receivers which can operate only with SAW- or crystal-based transmitters. In sweep-mode, a range reduction will occur in installations where there is a strong interferer in the swept RF band. This is because the process indiscriminately includes all signals within the sweep range. A CY801 may be used in place of a super-regenerative receiver in most applications.

Step B: Selecting the Reference Oscillator

All timing and tuning operations on the CY801 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of three ways:

1) Connect a ceramic resonator
2) Connect a crystal
3) Drive this pin with an external timing signal

The specific reference frequency required is related to the system transmit frequency and to the operating mode of the receiver as set by the SWEN pin.

B.1 Crystal or Ceramic Resonator Selection

Do not use resonators with integral capacitors since capacitors are included in the IC, also

care should be taken to ensure low ESR capacitors are selected. If operating in fixed-mode, a crystal is recommended. In sweep-mode either a crystal or ceramic resonator may be used. When a crystal of ceramic resonator is used the minimum voltage is 300mVPP. If using an externally applied signal it should be AC-coupled and limited to the operating range of 0.1VPP to 1.5VPP.

B.2 Selecting Reference Oscillator Frequency fT (Fixed Mode)

As with any super-heterodyne receiver, the mixing between the internal LO (local oscillator) frequency f_{LO} and the incoming transmit frequency f_{TX} ideally must equal the IF center frequency.

Equation 1 may be used to compute the appropriate f_{LO} for a given f_{TX}:

(1) $$f_{LO} = f_{TX} \pm \left(0.86 \frac{f_{TX}}{315}\right)$$

Frequencies f_{TX} and f_{LO} are in MHz. Note that two values of f_{LO} exist for any given f_{TX}, distinguished as "high-side mixing" and "low-side mixing." High-side mixing results in an image frequency above the frequency of interest and low-side mixing results in a frequency below.

After choosing one of the two acceptable values of f_{LO}, use Equation 2 to compute the referenceoscillator frequency f_T:

(2) $$f_T = \frac{F_{LO}}{64.5}$$

Frequency f_T is in MHz. Connect a crystal of frequency f_T to REFOSC on the CY801. Four-decimal-place accuracy on the frequency is generally adequate. The following table identifies f_T for some common transmit frequencies when the CY801 is operated in fixe mode.

Transmit Frequency (f_{TX})	Reference Oscillator Frequency (f_T)
315MHz	4.8970MHz
390MHz	6.0630MHz
418MHz	6.4983MHz
433.92MHz	6.7458MHz

Table 1. Fixed-Mode Recommended Reference Oscillator Values For Typical Transmit Frequencies (high-side mixing)

Selecting REFOSC Frequency fT (Sweep Mode)

Selection of the reference oscillator frequency f_T in sweep mode is much simpler than in fixed mode due to the LO sweeping process. Also, accuracy requirements of the frequency reference component are significantly relaxed.

In sweep mode, f_T is given by Equation 3:

(3) $$f_T = 2 \times \frac{f_{TX}}{64.25}$$

In sweep mode a reference oscillator with frequency accurate to two-decimal-places is generally adequate. A crystal may be used and may be necessary in some cases if the transmit frequency is particularly imprecise.

Transmit Frequency (f_{TX})	Reference Oscillator Frequency (f_T)
315MHz	9.76MHz
390MHz	12.10MHz
418MHz	12.96MHz
433.92MHz	13.46MHz

Table 2. Sweep-Mode Recommended Reference Oscillator Values For Typical Transmit Frequencies

Step C: Selecting the CTH Capacitor

Extraction of the dc value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor CTH and the on-chip switched-capacitor "resistor" RSC, shown in the block diagram. Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typically values range from 5ms to 50ms. Optimization of the value of CTH is required to maximize range.

C.1 Selecting Capacitor CTH

The first step in the process is selection of a

data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure (that is, existence of data preamble, etc.).

The effective resistance of R_{SC} is listed in the electrical characteristics table as 145kΩ at 315MHz, this value scales linearly with frequency. Source impedance of the CTH pin at other frequencies is given by equation (4), where f_T is in MHz:

(4) $$R_{SC} = 145k\Omega \frac{4.8970}{f_T}$$

τ of 5x the bit-rate is recommended. Assuming that a slicing level time constant τ has been established, capacitor CTH may be computed using equation

(5) $$C_{TH} = \frac{\tau}{R_{SC}}$$

A standard ±20% X7R ceramic capacitor is generally sufficient. Refer to Application Hint 42 for C_{TH} and C_{AGC} selection examples.

Step D: Selecting the C_{AGC} Capacitor

The signal path has AGC (automatic gain control) to increase input dynamic range. The attack time constant of the AGC is set externally by the value of the C_{AGC} capacitor connected to the CAGC pin of the device. To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under 10mVpp once the control voltage has attained its quiescent value. For this reason capacitor values of at least 0.47µF are recommended.The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the CY801. When the device is placed into shutdown mode (SHUT pin pulled high), the AGC capacitor floats to retain the voltage. When operation is resumed, only the voltage droop due to capacitor leakage must be replenished. A relatively low-leakage capacitor is recommended when the devices are used in duty-cycled operation. To further enhance duty-cycled operation, the AGC push and pull currents are boosted for approximately 10ms immediately after the device is taken out of shutdown. This compensates for AGC capacitor voltage droop and reduces the time to restore the correct AGC voltage. The current is boosted by a factor of 45.

D.1 Selecting C_{AGC} Capacitor in Continuous Mode

A C_{AGC} capacitor in the range of 0.47µF to 4.7µF is typically recommended. The value of the C_{AGC} should be selected to minimize the ripple on the AGC control voltage by using a sufficiently large capacitor. However if the capacitor is too large the AGC may react too slowly to incoming signals. AGC settling time from a completely discharged (zero-volt) state is given approximately by Equation 6:

(6) $\Delta t = 1.333 C_{AGC} - 0.44$

Where: C_{AGC} is in µF, and Δt is in seconds.

D.2 Selecting CAGC Capacitor in Duty-Cycle Mode

Voltage droop across the C_{AGC} capacitor during shutdown should be replenished as quickly as possible after the IC is enabled. As mentioned above, the CY801 boosts the push-pull current by a factor of 45 immediately after start-up. This fixed time period is based on the reference oscillator frequency f_T. The time is 10.9ms for f_T = 6.00MHz, and varies inversely with f_T. The value of C_{AGC} capacitor and the duration of the shutdown time period should be selected such that the droop can be replenished within this 10ms period. Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. Worst-casefrom a recovery standpoint is downward droop, since the AGC pull-up current is 1/10th magnitude of the pulldown current. The downward droop is replenished

according to the Equation 7:

(7) $$\frac{I}{C_{AGC}} = \frac{\Delta V}{\Delta t}$$

Where:

I = AGC pullup current for the initial 10ms (67.5μA)

C_{AGC} = AGC capacitor value

Δt = droop recovery time

ΔV = droop voltage

For example, if user desires Δt = 10ms and chooses a 4.7μF C_{AGC}, then the allowable droop is about 144mV. Using the same equation with 200nA worst case pin leakage and assuming 1μA of capacitor leakage in the same direction, the maximum allowable Δt (shutdown time) is about 0.56s for droop recovery in 10ms.

The ratio of decay-to-attack time-constant is fixed at 10:1 (that is, the attack time constant is 1/10th of the decay time constant). Generally the design value of 10:1 is adequate for the vast majority of applications. If adjustment is required the constant may be varied by adding a resistor in parallel with the C_{AGC} capacitor. The value of the resistor must be determined on a case by case basis.

Step E: Selecting the Demod Filter Bandwidth

The inputs SEL0 and SEL1 control the demodulator filter bandwidth in four binary steps (625Hz to 5000Hz in sweep, 1250Hz to 8000Hz in fixed mode), see Table 3. Bandwidth must be selected according to the application. The demodulator bandwidth should be set according to equation 8.

(8) $$\text{Demodulator Bandwidth} = \frac{0.65}{\text{shortest pulse-width}}$$

It should be noted that the values indicated in table 1 are nominal values. The filter bandwidth scales linearly with frequency so the exact value will depend on the operating frequency. Refer to the "Electrical Characteristics" for the exact filter bandwidth at a chosen frequency.

SEL0	SEL1	Demodulator Bandwidth	
		Sweep Mode	Fixed Mode
1	1	4000Hz	8000Hz
0	1	2500Hz	5000Hz
1	0	1250Hz	2500Hz
0	0	625Hz	1250Hz

Table 3. Nominal Demodulator Filter Bandwidth vs. SEL0, SEL1 and Operating Mode

For SYN800, the pins of SEL0 and SEL1 are connected to ground. For SYN801, its are determined by customer.

Crystal is the reference clock for all the device internal circuits. Crystal characteristics of 20pF load capacitance, 20ppm, ESR < 50Ω, -40ºC to +85ºC temperature range are desired. Table 4 shows the crystal frequencies and one of CY company approved crystal manufacturers.

The oscillator of the CY801 is a Colpitts type. It is very sensitive to stray capacitance loads. Thus, very good care must be taken when laying out the printed circuit board. Avoid long traces and ground plane on the top layer close to the REFOSC pin.

Crystal	Pack	Freq. MHz	Mode	Load	Tol.	Temp. Range	T. Stab.	ESR
HC-49/S Low Profile	Bulk	4.897	Fundam	20pF	±20 ppM	-40° to 85°	±20 ppM	≤60Ω

HC-49/S Low Profile	Bulk	6.7458	Fundam	20pF	±20 ppM	-40° to 85°	±20 ppM	≤60Ω

Table 4. Crystal Frequency and Vendor Part Number

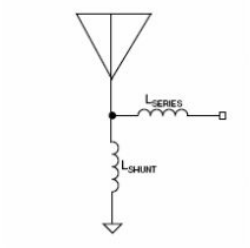
Antenna Impedance Matching

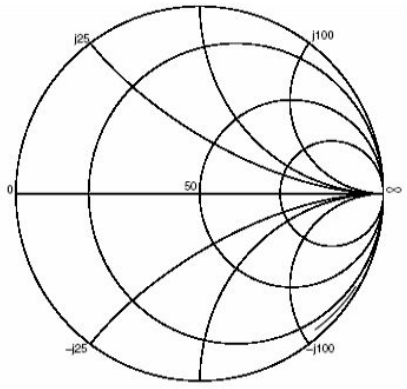
As shown in table 5 the antenna pin input impedance is frequency dependant.
The ANT pin can be matched to 50 Ohms with an L-type circuit. That is, a shunt inductor from the RF input to ground and another in series from the RF input to the antenna pin.
Inductor values may be different from table depending on PCB material, PCB thickness, ground configuration, and how long the traces are in the layout. Values shown were characterized for a 0.031 thickness, FR4 board, solid ground plane on bottom layer, and very short traces. MuRata and Coilcraft wire wound 0603 or 0805 surface mount inductors were tested, however any wire wound inductor with high SRF (self resonance frequency) should do the job.

Frequency （MHz）	ZIN() Z11	S11	LSHUNT(nH)	LSERIES(nH)
300	12-j166	0.803-j0.529	15	72
305	12-j165	0.800-j0.530	15	72
310	12-j163	0.796-j0.536	15	72
315	12-j162	0.791-j0.536	15	72
320	12-j160	0.789-j0.543	15	68
325	12-j157	0.782-j0.550	12	68
330	12-j155	0.778-j0.556	12	68
335	12-j152	0.770-j0.564	12	68
340	11-j150	0.767-j0.572	15	56
345	11-j148	0.762-j0.578	15	56
350	11-j145	0.753-j0.603	12	56
355	11-j143	0.748-j0.592	12	56
360	11-j141	0.742-j0.59	10	56
365	11-j139	0.735-j0.603	10	56
370	10-j137	0.732-j0.612	12	47
375	10-j135	0.725-j0.619	12	47
380	10-j133	0.718-j0.625	10	47
385	10-j131	0.711-j0.631	10	47
390	10-j130	0.707-j0.634	10	43
395	10-j128	0.700-j0.641	10	43
400	10-j126	0.692-j0.647	10	43
405	10-j124	0.684-j0.653	10	39
410	10-j122	0.675-j0.660	10	39
415	10-j120	0.667-j0.667	10	39
420	10-j118	0.658-j0.673	10	36
425	10-j117	0.653-j0.677	10	36
430	10-j115	0.643-j0.684	10	33

435	10-j114	0.638-j0.687	10	33
440	8-j112	0.635-j0.704	8.2	33

Table 5. Input Impedance Versus Frequency





Shutdown Function

Duty-cycled operation of the CY801 (often referred to as polling) is achieved by turning the CY801 on and off via the SHUT pin. The shutdown function is controlled by a logic state applied to the SHUT pin. When VSHUT is high, the device goes into low-power standby mode. This pin is pulled high internally; it must be externally pulled low to enable the receiver.

Power Supply Bypass Capacitors

VDDBB and VDDRF should be connected together directly at the IC pins. Supply bypass capacitors are strongly recommended. They should be connected to VDDBB and VDDRF and should have the shortest possible lead lengths. For best performance, connect VSSRF to VSSBB at the power supply only (that is, keep V_{SSBB} currents from flowing through the V_{SSRF} return path).

Increasing Selectivity with an Optional Band Pass Filter

For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and VSSRF to provide additional receive selectivity and input overload protection.

Data Squelching

During quiet periods (no signal) the data output (DO pin) transitions randomly with noise. Most decoders can discriminate between this random noise and actual data but for some system it does present a problem. There are three possible approaches to reducing this output noise:

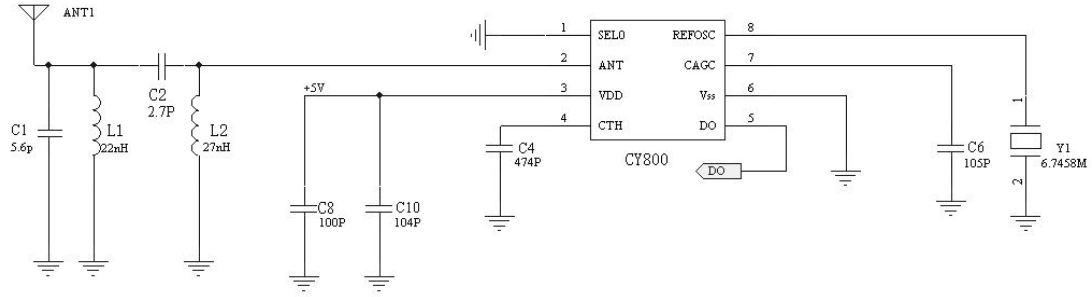
1) Analog squelch to raise the demodulator threshold

2) Digital squelch to disable the output when data is not present

3) Output filter to filter the (high frequency) noise glitches on the data output pin.

The simplest solution is add analog squelch by introducing a small offset, or squelch voltage, on the CTH pin so that noise does not trigger the internal comparator. Usually 20mV to 30mV is sufficient, and may be achieved by connecting a several-mega ohm resistor from the CTH pin to either V_{SS} or V_{DD}, depending on the desired offset polarity. Since the CY801has receiver AGC noise at the internal comparator input is always the same, set by the AGC. The squelch offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce sensitivity and also reduce range. Only introduce an amount of offset sufficient to quiet the output. Typical squelch resistor values range from 6.8MΩ to 10MΩ

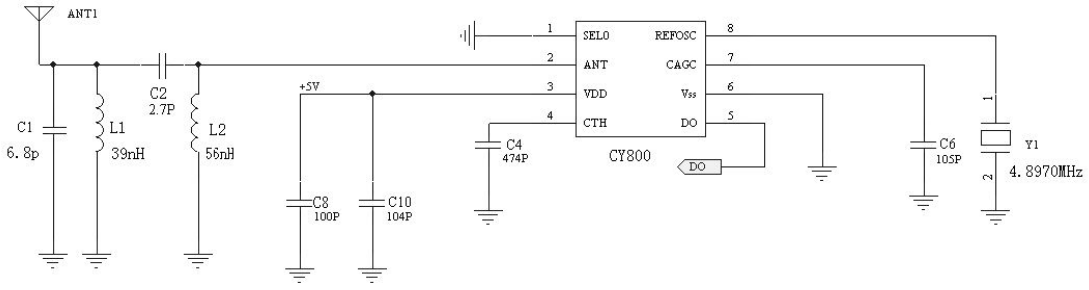
Schematic of CY800 Receiver Module @433.92MHz



BOM of CY800 @433.92 MHz

Item	Manufacturer	Description	Qty.
C1	MuRata	5.6pF , 0402/0603	1
C2	MuRata	2.7pF , 0402/0603	1
C4	MuRata	1uF , 0402/0603	1
C6	MuRata	1uF , 0402/0603	1
C8	MuRata	100pF , 0402/0603	1
C10	MuRata	0.1uF , 0402/0603	1
L1	MuRata	22nH 5%, 0402/0603	1
L2	MuRata	27nH 5%, 0402/0603	1
U1	CY800	SOP-8	1
Y1	CY6.7458MHz	HC49S	1

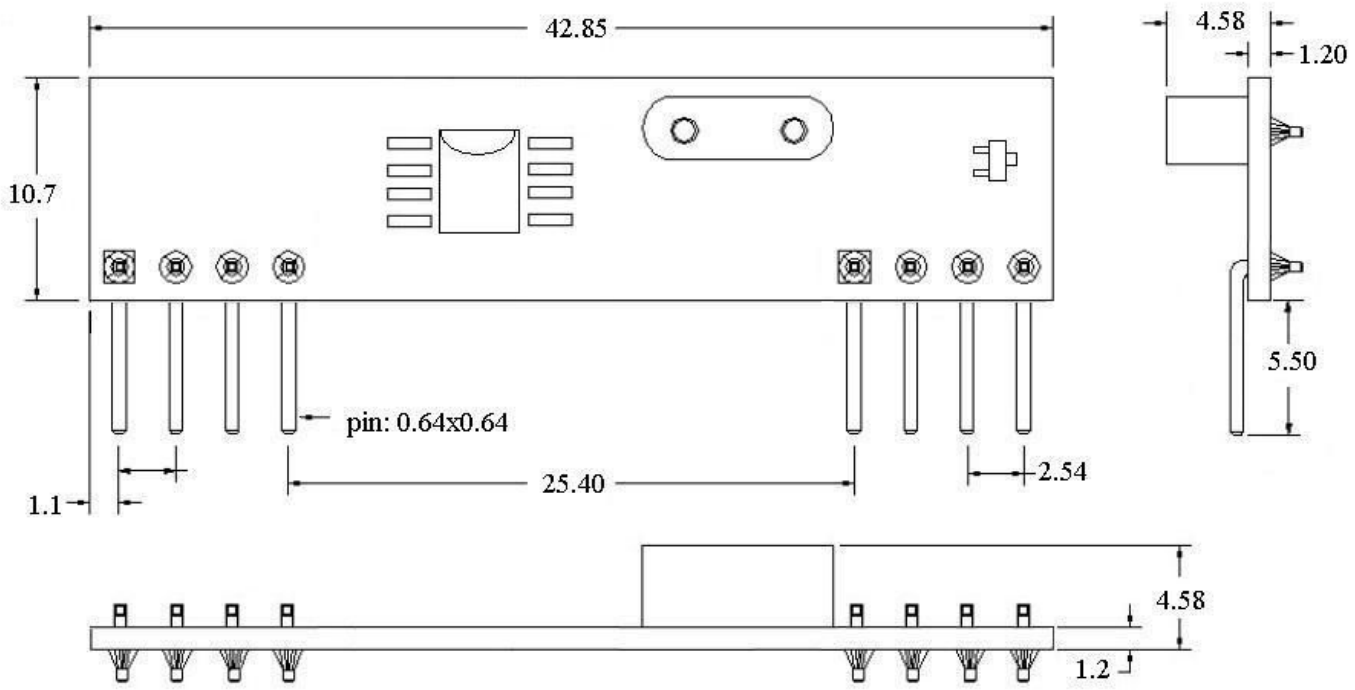
Schematic of CY800 Receiver Module @315MHz



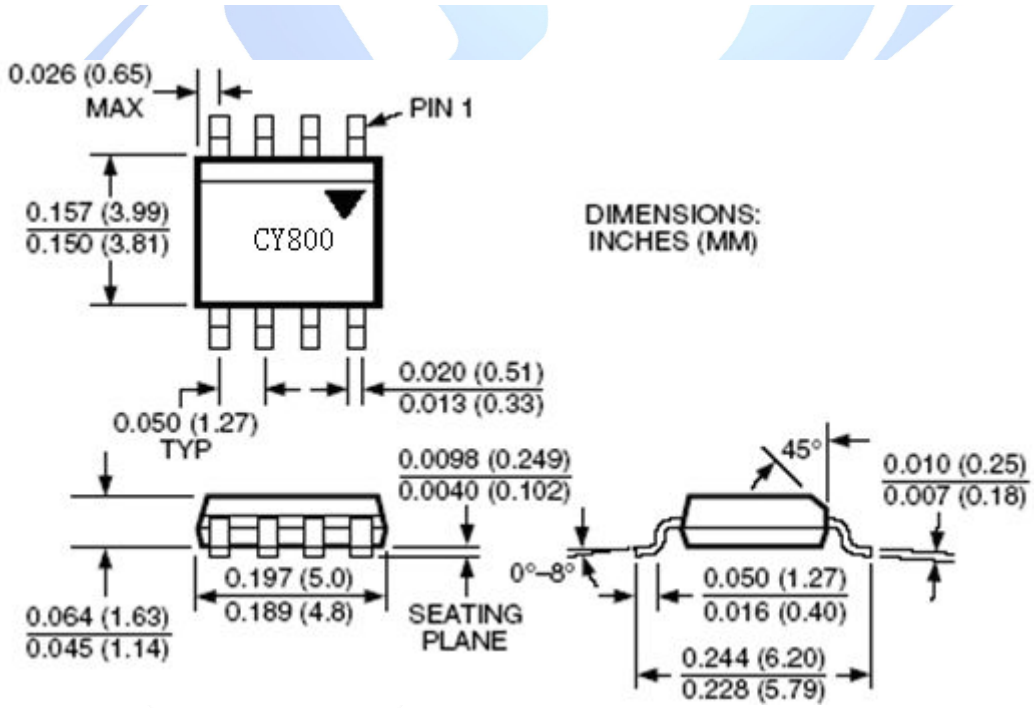
BOM of CY800 @315 MHz

Item	Manufacturer	Description	Qty.
C1	MuRata	6.8pF , 0402/0603	1
C2	MuRata	2.7pF , 0402/0603	1
C4	MuRata	1uF , 0402/0603	1
C6	MuRata	1uF , 0402/0603	1
C8	MuRata	100pF , 0402/0603	1
C10	MuRata	0.1uF , 0402/0603	1
L1	MuRata	39nH 5%, 0402/0603	1
L2	MuRata	56nH 5%, 0402/0603	1
U1	CY800	SOP-8	1
Y1	CY4.8970MHz	HC49S	1

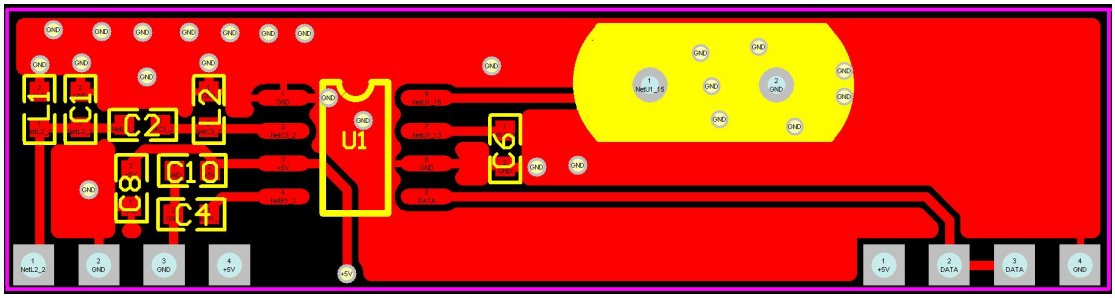
CY800 Module Mechanical Size: (unit: mm)

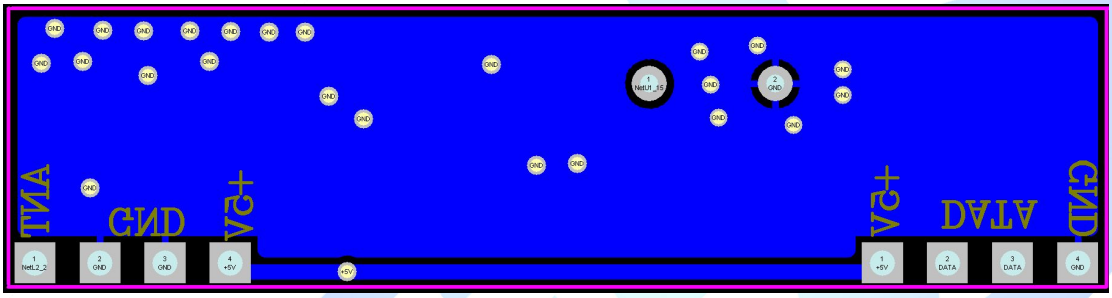


Package Information: (unit: mm)



CY800 PCB





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